Composition, structure, and electrical characteristics of HfO_2 gate dielectrics grown using the remote- and direct-plasma atomic layer deposition methods

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Hafnium oxide thin films were deposited using both the remote-plasma atomic layer deposition (RPALD) and direct-plasma atomic layer deposition (DPALD) methods. Metal-oxide semiconductor (MOS) capacitors and transistors were fabricated with HfO_2 gate dielectric to examine their electrical characteristics. The as-deposited RPALD HfO_2 layer exhibited an amorphous structure, while the DPALD HfO_2 layer exhibited a polycrystalline structure. Medium-energy ion scattering measurement data indicate that the interfacial layer consisted of interfacial SiO_{2-x} and silicate layers. This suggests that the change in stoichiometry with depth could be related to the energetic plasma beam used in the plasma ALD process, resulting in damage to the Si surface and an interaction between Hf and SiO_{2-x}. The as-deposited RPALD HfO_2 films had better interfacial layer characteristics, such as an effective fixed oxide charge density ($Q_{f,\mathrm{eff}}$) and interfacial roughness than the DPALD HfO_2 films did. A MOS capacitor fabricated using the RPALD method exhibited an equivalent oxide thickness (EOT) of 1.8 nm with a $Q_{f,\mathrm{eff}}=-4.2\times10^{11}\ q/\mathrm{cm}^2$ (where q is the elementary charge, 1.6022×10^{-19} C), whereas a MOS capacitor fabricated using the DPALD method had an EOT=2.0 nm and a $Q_{f,\mathrm{eff}}=-1.2\times10^{13}\ q/\mathrm{cm}^2$. At a power=0.6 MV/cm, the RPALD n-type metal-oxide semiconductor field-effect transistor (nMOSFET) showed $\mu_{\mathrm{eff}}=168\ \mathrm{cm}^2/\mathrm{V\ s}$, which was 50% greater than the value of the DPALD nMOSFET ($\mu_{\mathrm{eff}}=111\ \mathrm{cm}^2/\mathrm{V\ s}$). In the region where V_g-V_t=2.0 V, the RPALD MOSFET drain current was about 30% higher than the DPALD MOSFET drain current. These improvements are believed to be due to the lower effective fixed charge density, and they minimize problems arising from plasma charging damage. © *2005 American Institute of Physics*. [DOI: 10.1063/1.2121929]

I. INTRODUCTION

Alternative gate dielectric insulators with high dielectric constants (i.e., high k) are in demand because the aggressive demands of scaling of Si metal-oxide semiconductor (MOS) field-effect transistors (FETs) limit the use of SiO_2 as a gate dielectric insulator.[1] HfO_2 is one of the most promising high-k materials that have been proposed to replace SiO_2 gate dielectrics because of its high dielectric constant (k =18–25), its wide band gap/barrier height, and its good thermal stability.[2]

Atomic layer deposition (ALD) has been studied for depositing high-k materials, and has many practical advantages, such as precise thickness control at the nanolevel and the ability to grow uniform films over a large substrate area.[3–5] The ALD process employing halogen precursors provides good step coverage and a low impurity concentration in thin films.[6,7] However, several problems are associated with this method: (i) the presence of halogen atom residues in films, (ii) the corrosion of gas delivery lines, and (iii) the generation of particles. It has been suggested that ALD using metal organic precursors could overcome these problems.[8] Although the use of metal organic precursors has many advantages in growing films, some problems have been reported, such as low film densities and high impurity contamination.

To resolve these problems, the plasma-enhanced ALD (PEALD) method has been suggested to grow high-k thin films. The PEALD method is expected to increase the reactivity of the precursors, reduce impurities, widen the process window, and produce dense films. A variety of versatile

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PEALD precursors and reactants can be used, because of the high reactivity achieved in a plasma. For the above reasons, PEALD appears to be the key next generation deposition technology for semiconductor devices.[9] Although the PEALD method has many advantages for depositing high-*k* thin films, the effect of plasma damage on the deposited high-*k* film and substrate has not been extensively studied. In particular, high-energy particles in a plasma can induce damage, which results in the degradation of interface quality, inducing a high interface state density and a high fixed charge.[10] A degraded interface reduces carrier mobility and lowers the operating speed of a device.[11] Therefore, it is necessary to examine thoroughly the plasma damage in a gate structure and measures to suppress it.[12,13]

On the other hand, the application of metal gate and high dielectric constant gate dielectrics to MOSFET fabrication is an important issue in the sub-100 nm regime, because metal gate and high gate dielectric technology can realize (i) a low gate resistance (i.e., a high-speed device), (ii) no gate depletion (i.e., reduction of the electrical gate oxide thickness), (iii) no boron penetration from the gate into the channel, and (iv) low gate leakage current, i.e., we can obtain continuous transistor scaling and device performance improvement.[14–16] However, metal gate and high dielectric constant materials are easily degraded by high-temperature processes, such as activation annealing used for source/drain formation ($T \sim 1000\ ^\circ\mathrm{C}$).[14]

To overcome these problems and to compare the intrinsic properties of HfO_2 prepared using two different plasma-assisted ALD methods, we have fabricated *n*-type metal-oxide semiconductor field-effect transistors (nMOSFETs) using a replacement gate process in which the gate dielectrics and the metal gate were fabricated after source/drain formation at high temperatures.[17] The HfO_2 gate dielectric was prepared using the RPALD and DPALD methods employing tetrakis diethylaminohafnium (TDEAH) and an O_2 plasma. After deposition of the HfO_2 films using these two different PEALD methods, we investigated the composition, structure, and electrical characteristics of the films. In addition, the characteristics of nMOSFET devices with HfO_2 gate dielectrics grown using these two different PEALD methods were studied.

II. EXPERIMENT

The HfO_2 thin films were deposited on *p*-type Si substrates with ⟨100⟩ orientation and a resistivity in the range of 6–12 Ω cm. The HfO_2 films had a thickness of about 5.0 nm and were prepared using a substrate temperature of 250 °C. Before HfO_2 deposition, the Si substrates were cleaned in dilute HF solution (1% HF) to remove any surface oxide and other residue. The hafnium precursor, TDEAH, was introduced into the ALD chamber via a bubbler using argon carrier gas. The oxygen reactant was produced during pulsing of the O_2 plasma. The basic one cycle consisted of supplying the hafnium precursor and the oxygen plasma as a source and a reactant gas, respectively. Argon purge gas was introduced for the complete separation of the precursor and reactant gas.

The thickness of the films was determined from cross sections using high-resolution transmission electron microscopy (HRTEM). The chemical composition of the as-deposited HfO_2 films was studied using x-ray photoelectron spectroscopy (XPS) and medium-energy ion scattering (MEIS), respectively. The MEIS analysis was accomplished using a 100 keV proton beam in a double alignment that reduced contributions from the crystalline Si substrate, and permitted the deconvolution of the spectra into contributions from the interfacial layer and Si. The incident ions were directed along the Si (111) plane, and the scattered ions were directed along the Si (001) plane at a scattering angle of 125°. Quantitative depth profiles for the different species were extracted at a resolution of <0.5 nm near the surface.[10]

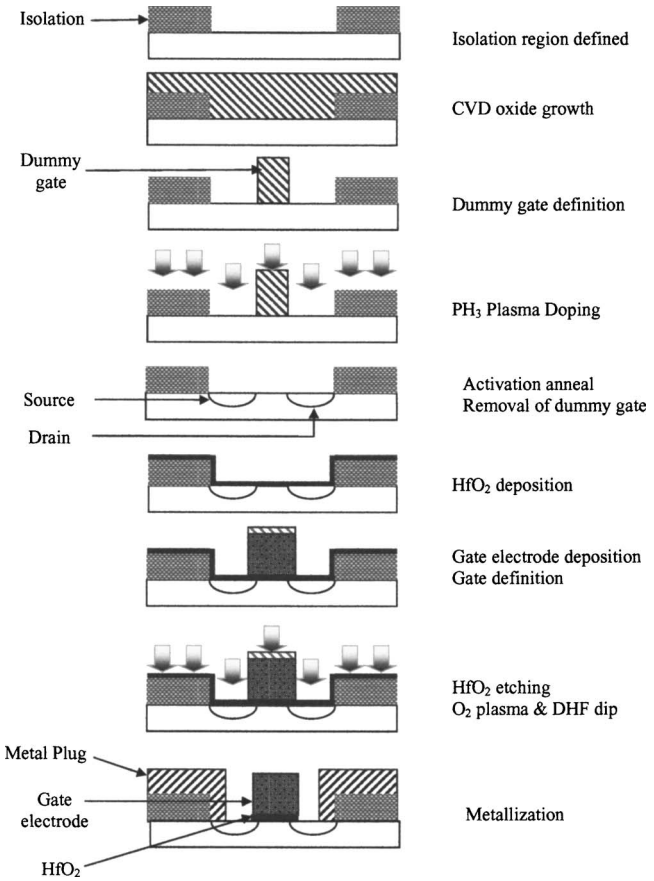

FIG. 1. The replacement gate nMOSFET fabrication process.

The MOS capacitors were fabricated with a HfO_2 thickness of 5.0 nm and a Pt electrode thickness of 100 nm. For postdeposition annealing, the substrate was rapidly annealed at 800 °C for 10 s in a N_2 atmosphere. A postmetallization anneal was also carried out in a hydrogen- and nitrogen-mixed atmosphere at 450 °C for 30 min. The capacitance-voltage (*C-V*) characteristics of the HfO_2 MOS capacitors were measured using a Keithley 590 analyzer.

The nMOSFETs with the HfO_2 gate dielectrics were prepared employing the replacement gate process. Figure 1 shows a schematic diagram of the process. The isolation region was formed by thermal oxidation and wet etching using a buffered oxide etcher (BOE). The dummy gate region for the formation of the source/drain (S/D) region was formed using a low-temperature chemical vapor deposition (CVD) oxide. PH_3 plasma doping and rapid annealing at 950 °C

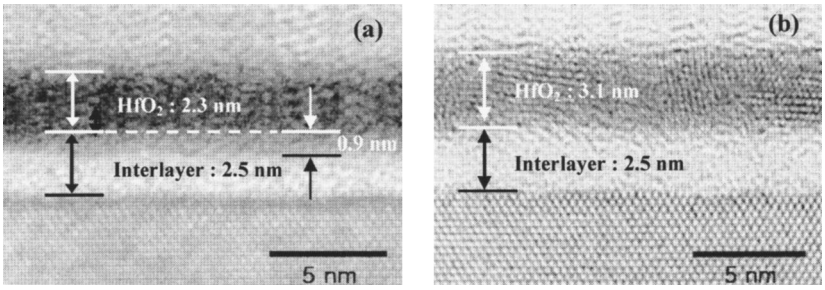

FIG. 2. A cross-sectional HRTEM micrograph of as-grown HfO_2 films deposited on a Si substrate using (a) the RPALD and (b) the DPALD methods at a deposition temperature of 250 °C using $Hf(NEt_2)_4$ precursor.

were used to form the S/D region. After the S/D activation annealing, the dummy gate oxide was removed by wet etching. During the wet etching of the CVD oxide, the S/D region maintained a low electrical resistance, which meant that the S/D region was not affected by the etching process. The thickness of the HfO_2 gate dielectrics was prepared about 5.0–6.0 nm. The gate electrode chosen was an Al/TaN stack grown using the dc magnetron sputtering technique. After the gate region definition, followed by metallization, the electrical characteristics of nMOSFETs were evaluated using a Hewlett Packard HP 4155 parameter analyzer and an HP 4282 *LCR* meter.

III. RESULTS AND DISCUSSION

A. High-resolution transmission electron microscopy

Figure 2 shows the HRTEM micrographs of as-deposited HfO_2 films prepared using the RPALD and the DPALD methods. From the contrast in the TEM micrographs, the thickness of the interfacial layer in the samples was approximately the same, whereas the thickness of the DPALD HfO_2 layer (3.1 nm) without an interfacial layer was thicker than that of the RPALD HfO_2 layer (2.3 nm). The change in contrast in moving from the interfacial layer to the HfO_2 layer of the RPALD film was gradual, including the change in passing through the transition layer, whereas the contrast in the DPALD film changed abruptly when passing from the interfacial layer to the HfO_2 layer.

In general, a reaction in the interfacial layer depends on the energetic species of the plasma because this affects the mixing of atoms and chemical reactions occurring near to the substrate by influencing the transfer of momentum and diffusion.[18] The thickness and stoichiometry of the interfacial layer were checked using MEIS, and will be discussed later. We also observed that the as-deposited RPALD HfO_2 layer was amorphous, whereas the as-deposited DPALD HfO_2 layer was polycrystalline. The HfO_2 thin film with a thickness of <5.0 nm grown using the ALD process without a plasma was reported to have an amorphous structure.[10] However, in our DPALD films having a 3-nm-thick HfO_2 layer, the films became partially crystallized [as shown in Fig. 2(b)]. This is because the metastable species in the plasma can release their energy through collisions, and this can result in crystallization.[18] Therefore, we consider that the crystallization in the DPALD sample was induced as the result of an enhanced physical reactivity of the oxygen ions in the plasma.

B. X-ray photoelectron spectroscopy

Figure 3 shows the XPS spectra of the as-deposited HfO_2 samples. A difference in the Hf $4f_{7/2}$ peak position between the RPALD and DPALD HfO_2 films was observed, with binding energies of 16.6 eV for RPALD film and 17.6 eV for DPALD film, respectively, as shown in Fig. 3(a). Wilk *et al.* have reported that the Hf $4f_{7/2}$ peak of Hf silicate was ~1 eV higher in energy than the Hf $4f_{7/2}$ peak HfO_2, which is located at 16.5–17 eV.[19] Thus, the peak shift to higher binding energy for the DPALD sample indicates the formation of Hf silicate, implying that silicate formation was higher than in the RPALD sample. In Fig. 3(b), the Si $2p$ spectra showed a higher binding energy, which was the result of silicate and SiO_2 forming in the interfacial layer; the two samples exhibited different peak positions and intensity. These results indicate that the interfacial layers contained a Hf silicate layer, and that this had different thicknesses and stoichiometry in the two samples.

C. Medium-energy ion scattering measurements

The MEIS measurements were carried out to investigate the stoichiometry of the interfacial layer and its depth, as shown in Fig. 4. The molecular density of HfO_2 ($\sim 2.49 \times 10^{22}$ Hf atoms/cm^3) was used to extract the stoichiometry in the depth direction from the MEIS data to provide an area

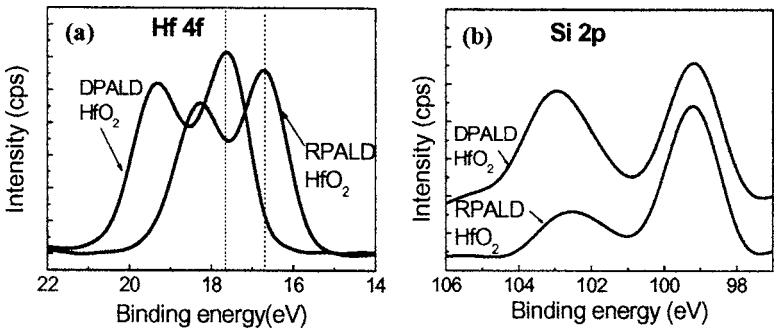

FIG. 3. XPS spectra of as-grown RPALD and DPALD samples showing (a) the Hf $4f$ and (b) Si $2p$ peaks. The HfO_2 films of the samples were grown using 50 ALD cycles and the plasma power of 100 W.

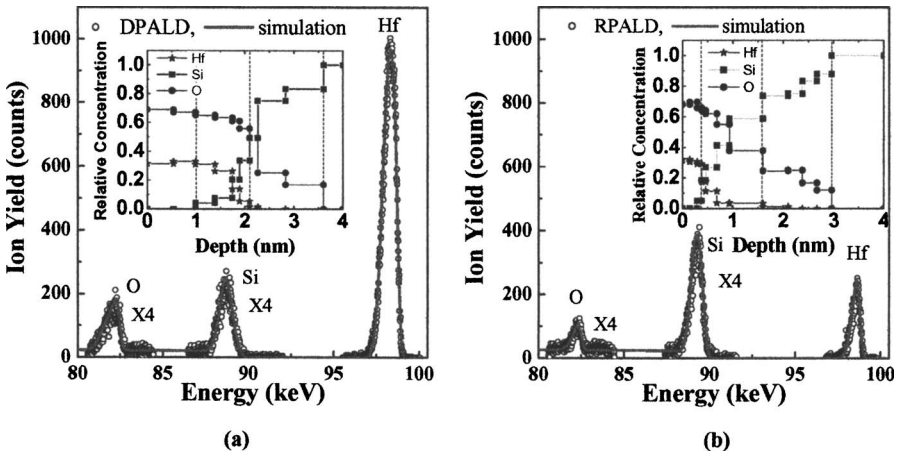

FIG. 4. MEIS results for (a) as-grown DPALD and (b) RPALD HfO_2 films. The open circles and solid lines represent raw data and fitted data, respectively. The inset shows the relative concentration along the depth direction of the films calculated from the fitted results.

density. We prepared a HfO_2 film with a thickness of about 4 nm to examine the damage caused to the Si substrate by the plasma charge, and to determine the chemical stoichiometry of the interfacial layer. The Hf peak spectra of the two samples show clear differences. The mass of Hf grown using the RPALD method was very low when compared with the mass of Hf grown using the DPALD method. This difference in mass of Hf grown suggests that the growth rate of HfO_2 using the DPALD method was higher than the growth rate of HfO_2 using the RPALD method. Since the mass of chemisorbed Hf during the first cycle was not dependent on the activity of the reactant in ALD growth when steric hindrance is considered, the difference in growth rate is related to the generated active sites that are able to react with the TDEAH molecules.

In general, an energetic plasma beam results in a change in the surface state of the Si, SiO_{2-x}, and HfO_2 layers to a more active site where the Hf source can react during the Hf supply period. It is also noteworthy that a difference in the stoichiometry of the interfacial layer in the depth direction is clearly observed between the two samples, as is shown by the fit of the data shown in Fig. 4, represented by the solid line. The thickness of the interfacial layer, including the oxygen deficient SiO_{2-x} and silicate layers, is almost the same in the two samples, whereas the stoichiometry of the silicate layer is very different. Thus, the Hf-rich silicate layer is formed in the DPALD process, and a Si-rich silicate layer is produced in the RPALD process. This suggests that the change in stoichiometry along the depth direction is related to the energy of the plasma beam, and this results in damage occurring to the Si surface, and allows for interactions to take place between the Hf and SiO_{2-x}. Although the thickness of the samples observed using MEIS was not consistent with the TEM data because the area density of the films used did not correlate with the ideal value, the relative difference in thickness clearly reflects the differences between the two samples.

D. Electrical properties of HfO_2 MOS capacitors

The characteristics of the interface and dielectric layers of the RPALD and DPALD samples were compared by fabricating MOS capacitors having a top Pt electrode. Figure 5 shows high-frequency *C-V* curves measured at $f=1$ MHz for these MOS capacitors both before and after annealing at 800 °C. The equivalent oxide thickness (EOT) and flatband voltage (V_{fb}) were determined from the high-frequency *C-V* data in the strong accumulation region with a correction for quantum-mechanical effects.[20] Assuming that the mean position of the charge distribution in the film was located at the bottom of the interface, then the measured shift in V_{fb} can be converted into an effective fixed charge density of the dielectric stack, $Q_{f,\mathrm{eff}}$. The gate voltage was swept from accumulation to inversion and then back again. After annealing at 800 °C, the hystereses observed in the RPALD and DPALD samples were ~20 and 80 mV, respectively. In these capacitors, 10 mV corresponded to a $Q_{f,\mathrm{eff}}=\sim 1\times 10^{11}\ q/\mathrm{cm}^2$ (where q is the elementary charge, 1.6022×10^{-19} C. Table I summarizes the electrical properties of the MOS capacitor data shown in Fig. 5. The value of $Q_{f,\mathrm{eff}}$ can be related to the observed value of V_{fb} by the expression

$$V_{fb}=\Phi_{ms}\pm\frac{Q_{f,\mathrm{eff}}}{C_{acc}}, \tag{1}$$

where Φ_{ms} is the difference in work function between the Pt electrode and the Si substrate, and C_{acc} is the maximum accumulation capacitance. Thus, $Q_{f,\mathrm{eff}}$ can be determined from the observed values of V_{fb}, Φ_{ms}, and C_{acc}. To determine the value of Φ_{ms} in our MOS samples, the effective work function of Pt was set to 5.6 V, and the doping concentration of the *p*-type Si substrate was determined to be $5\times 10^{15}/\mathrm{cm}^2$. Then, Φ_{ms} (or the ideal V_{fb}) was calculated to be 0.62 V.

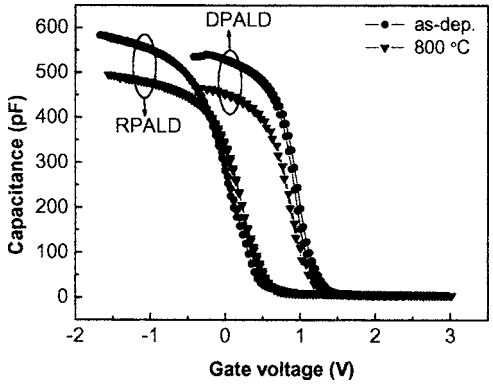

FIG. 5. Capacitance-voltage (*C-V*) curves for as-grown and annealed HfO_2 films deposited using the RPALD and DPALD methods.

TABLE I. Summary of the electrical properties of HfO_2 films deposited using the RPALD and DPALD methods.

Film treatment	Hysteresis (mV)	C_{acc} (pF/μm^2)	EOT (nm)	V_{fb} (V)	$Q_{f,eff}$ (q/cm^2)
RPALD-As	50	602	1.5	0.51	1.6×10^{12}
RPALD-800 °C	20	510	1.8	0.58	4.2×10^{11}
DPALD-As	120	543	1.6	1.33	-1.4×10^{13}
DPALD-800 °C	80	472	2.0	1.25	-1.2×10^{13}

The EOT of the RPALD sample was less than the EOT of the DPALD sample due to a difference in the film thickness, as shown in the TEM micrographs in Fig. 2, and the MEIS data in Fig. 5. After annealing at 800 °C, the EOT of each sample increased because of the decreased series capacitance of the increased thickness of the interfacial layer. The V_{fb} of the RPALD sample approached the ideal value of $V_{fb}=0.62$ V, more than did the value of V_{fb} of the DPALD sample. After annealing at 800 °C, the value of V_{fb} for both samples shifted towards the ideal $V_{fb}=0.62$ V. In the RPALD samples, $Q_{f,eff}$ decreased from 1.6×10^{12} to 4.2×10^{11} q/cm^2 as a result of the annealing process. In the DPALD samples, the value of $Q_{f,eff}$ decreased from -1.4×10^{13} to -1.2×10^{13} q/cm^2.

Most of the interface states are empty in the case of MOS capacitor on a *p*-type substrate at V_{fb}. Assuming the interface traps in the upper (lower) half of the band gap are acceptor- (donor-) type traps, then the acceptor-type (neutral when empty) interface traps above the Fermi energy (E_F) and the donor-type (positive when empty) interface traps below E_F do not contribute to the interface-trapped charge (Q_{it}) because they are both neutral. Further, the donor-type interface traps above E_F appear as a positive Q_{it}. The $Q_{f,eff}$ value is the sum of the true Q_f value and Q_{it}. Since Q_{it} is positive for *p*-type MOS capacitors, the true Q_f value of the DPALD sample would be a more negative value than the determined value of $Q_{f,eff}$($Q_{f,eff}=-1.2\times10^{13}$ q/cm^2). For the RPALD sample, the true Q_f value would be dependent on the relative magnitude and sign of $Q_{f,eff}$ and Q_{it}.[15] The true Q_f value of the annealed RPALD sample will be $\sim10^{11}$ q/cm^2, considering the calculated $Q_{f,eff}=4.2\times10^{11}$ q/cm^2.[21] Yeo *et al.* reported that the effective work function of Pt in a $Pt/HfO_2/Si$ structure was 5.3 V.[22] In our work, the ideal V_{fb} value for the MOS samples would be 0.32 V, instead of the 0.62 V used in Table I. Using this ideal V_{fb} value, the *C-V* curves shown in Fig. 5 indicate a negative value of $Q_{f,eff}$ for all the MOS samples. Nevertheless, the DPALD samples still had a more negative true Q_f value than the RPALD samples did. These large negative fixed oxide charges of the DPALD samples represent the negative charging effect due to the direct plasma process.

E. Characteristics of an Al/TaN metal gate nMOSFET

In this section, we compare the electrical properties of HfO_2 films grown using the RPALD and DPALD methods through the performance of two nMOSFETs with Al/TaN gate electrodes that were fabricated using the replacement gate process to reduce plasma and thermal damage. The effective width and length of the nMOSFETs were about 10.0 μm.

Figures 6(a) and 6(b) show cross-sectional TEM micrographs of nMOSFETs with HfO_2 gate dielectrics fabricated using the RPALD and DPALD methods, respectively. The physical thickness of the HfO_2 gate dielectric was 5.0–6.0 nm. As shown in Fig. 6, the interface between the Si substrate and the RPALD HfO_2 gate dielectric was much smoother than that of the DPALD sample. The observed rough interface of the DPALD sample increased the carrier scattering, as the electrons drifted from the source to the drain and, therefore, this reduced the channel mobility.

The RPALD nMOSFET showed a higher channel mobility than the DPALD nMOSFET. At 0.6 MV/cm, the μ_{eff} of the RPALD nMOSFET ($\mu_{eff}=168$ cm^2/V s) was 50% more than the μ_{eff} of the DPALD nMOSFET ($\mu_{eff}=111$ cm^2/V s). The degradation of the mobility in the DPALD nMOSFET relative to the RPALD nMOSFET can be attributed to electron scattering by the Coulomb-like potential because of the fixed charges near the interface in the inversion region and the increase in Coulumbic scattering

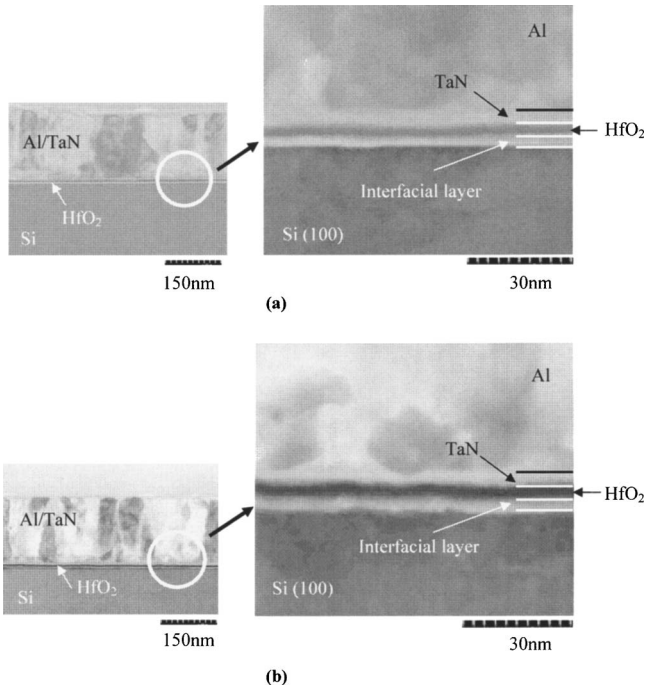

FIG. 6. Cross-sectional TEM micrographs of replacement Al/TaN-gate nMOSFETs with HfO_2 gate dielectrics grown using (a) the RPALD and (b) the DPALD methods. The effective width and length of the two nMOSFETs were about 10.0 μm.

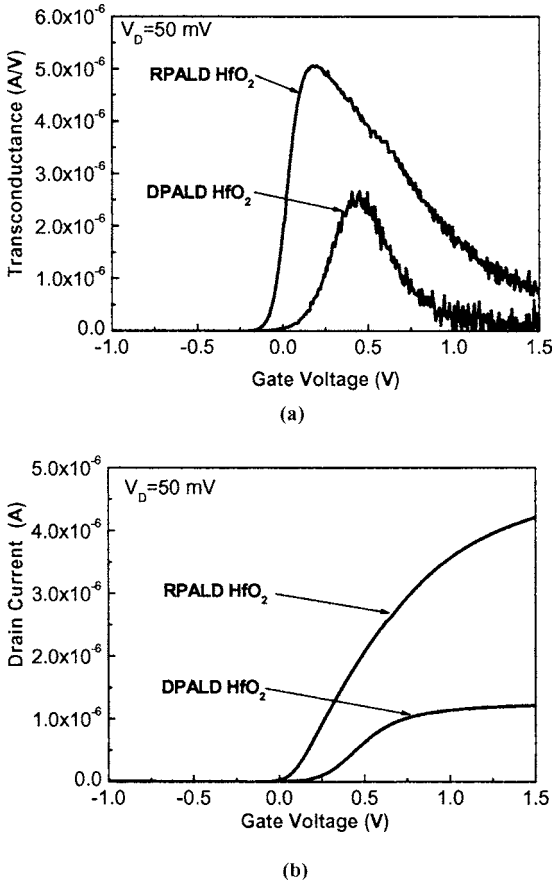

FIG. 7. The transconductance vs gate voltage (G_m-V_g) and drain current vs gate voltage curves (I_d-V_g) of replacement Al/TaN-gate nMOSFETs with HfO_2 gate dielectrics.

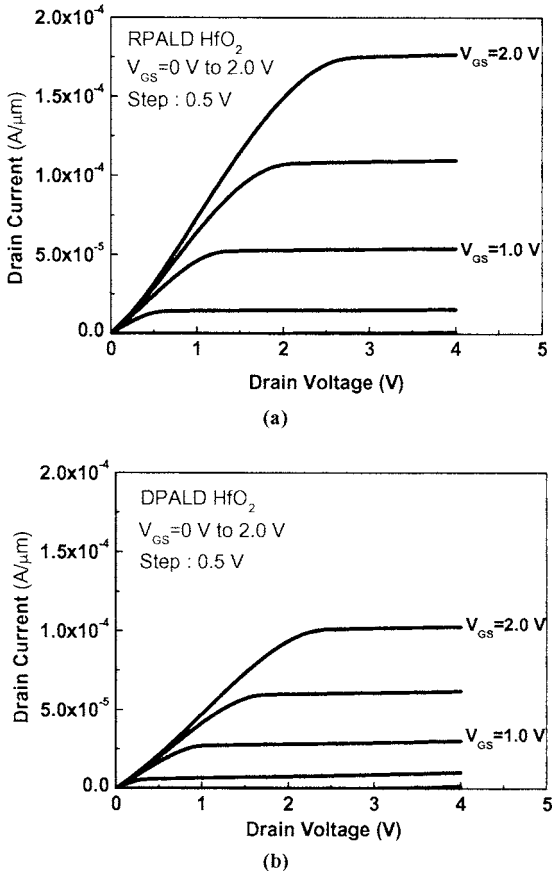

FIG. 8. Drain current vs drain voltage curves of Al/TaN replacement gate nMOSFETs with HfO_2 gate dielectrics grown using (a) the RPALD and (b) the DPALD methods. V=0 to 2.0 V. Step=0.5 V.

from the higher fixed oxide density in the HfO_2 film of the DPALD nMOSFET. Therefore, the high fixed charge density in the DPALD HfO_2 induced a loss of inversion charge in the channel, resulting in the degradation of electron mobility. In addition, as shown in Fig. 6, a microscopically rough interface between the oxide layer and the Si substrate in the DPALD nMOSFET can also cause scattering.

Comparisons of the transconductance (G_m) versus gate voltage (G_m-V_g) and drain current versus gate voltage (I_d-V_g) curves are shown in Figs. 7(a) and 7(b), respectively. As shown in Fig. 7(a), the transconductance of the RPALD nMOSFET was higher than the transconductance of the DPALD nMOSFET. In the I_d-V_g curves of the same nMOSFETs shown in Fig. 7(b), the subthreshold slope (sub-V_t) and the threshold voltage (V_t) were 85 mV/decade and 0.02 V, respectively, for the RPALD nMOSFET and 160 mV/decade and 0.30 V, respectively, for the DPALD nMOSFET. The value of V_t was derived from the extrapolated slope of the linear I_d vs V_g plot, at a value of the gate voltage (V_g) where the value of G_m (the differential of the I_d vs V_g curve) reaches a local maximum. The higher G_m and lower sub-V_t values indicate that the RPALD nMOSFET has better HfO_2/Si interface characteristics than the DPALD nMOSFET. The decrease in $|V_t|$ of the RPALD nMOSFET also seems to be the result of a reduction in the fixed oxide charges.

Figure 8 shows the output characteristics of HfO_2 gate dielectric nMOSFET with a gate bias between 0 and 2 V. Both the RPALD and DPALD nMOSFET devices showed good gate controlled linear and saturation regimes. In the region where V_g-V_t=2.0 V, the drain current in the RPALD nMOSFET was about 30% higher than the drain current in the DPALD nMOSFET device. The drain current was proportional to the carrier mobility.[23] Therefore, these improvements are achieved by reducing the degradation in mobility under normal fields, as shown in Figs. 9 and 7.

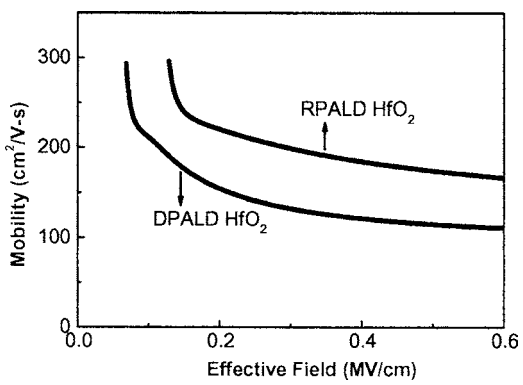

FIG. 9. Effective mobility as a function of effective electric field for replacement Al/TaN-gate nMOSFETs with HfO_2 gate dielectrics.

IV. CONCLUSIONS

The effect of remote-plasma and direct-plasma ALD processing on HfO_2 gate dielectric insulators was investigated. The as-deposited RPALD HfO_2 layer had an amorphous structure, whereas the as-deposited DPALD HfO_2 layer had a polycrystalline structure. The MEIS data indicate that the change in stoichiometry with depth is related to the energy of the plasma beam used in the ALD process. This results in damage to the Si surface, and allows for interactions between the Hf and SiO_{2-x}. The remote-plasma ALD method minimizes the problems caused by the use of a direct plasma.

The as-deposited RPALD HfO_2 films had better interfacial layer characteristics than the as-deposited DPALD HfO_2 films. The effective fixed oxide charge density was less for RPALD HfO_2 films than for DPALD HfO_2 films. The observed lower effective mobility of DPALD transistors versus RPALD transistors was due to electrons in the channel being scattered by the surface roughness and by Coulombic interactions with the large fixed charge density of the HfO_2 layer of DPALD transistors. This improvement was due to the lower effective fixed charge density, and the minimization of the damage caused by plasma charging. The interfacial roughness of the DPALD MOSFET led to carrier mobility degradation. In the region where V_g-V_t=2.0 V, the RPALD MOSFET drain current was about 30% higher than the DPALD MOSFET drain current.

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