Electronic structure of pentacene/ultrathin gate dielectric interfaces for low-voltage organic thin film transistors

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(Received 30 April 2007; accepted 24 July 2007; published online 17 September 2007)

This paper describes the fabrication of pentacene-based thin film transistors (TFTs) with ultrathin (4.5 nm) SiO_2 and SiON gate dielectric layers for low-voltage operations. The device with the SiON gate dielectric layer operated at gate voltages lower than −3.0 V, showing a threshold voltage of −0.45 V, which was lower than the threshold voltage of the SiO_2 device (−2.5 V). The electronic structures of the interface between the pentacene and dielectric layers were investigated by *in situ* ultraviolet photoelectron spectroscopy (UPS) and x-ray photoelectron spectroscopy (XPS) to determine the reason for the lower operating voltage. The UPS and XPS results demonstrated that the interface dipole modified the potential of the dielectric layer, explaining the lower operating voltage. The electronic structure allowed for band bending at the interface, resulting in complete energy level diagrams for pentacene on SiO_2 and SiON. The shifts in the threshold and turn-on voltages were explained by the energy level diagrams. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2779264]

I. INTRODUCTION

Organic thin film transistors (OTFTs) are widely used in practical applications such as flexible displays, pliable electronic paper, radio-frequency identification tags, and smart cards.[1–7] Important developments in materials and device structures have allowed organic semiconductors to replace the traditional inorganic semiconductors in these practical applications. However, the operating voltage required for OTFTs is too high for practical use. Accordingly, development of low-voltage operating OTFTs has become a priority. Recently, low-voltage driven OTFTs that use high-*k* metal oxides,[8,9] organic gate dielectrics,[10,11] and double gate dielectric layers[12,13] have been reported. The control of the threshold voltage during low-voltage operation depends, not only on the gate dielectric constants, but also on the interfacial electronic structures between the dielectric layers and the organic semiconductors. In this study, the fabrication of pentacene-based TFTs with ultrathin (4.5 nm) SiO_2 and SiON gate insulator films is described. SiO_2 is used widely as a gate dielectric in commercial thin film transistors. With extensive knowledge of the behavior of such devices, SiO_2 is also commonly used as a dielectric for OTFTs. However, attempts to reduce the thickness of SiO_2 to less than 2 nm have clearly demonstrated the limitations of SiO_2: high leakage current and poor resistance to boron penetration. Therefore, nitrided silicon dioxide (SiON) has replaced the conventional SiO_2 in dielectric applications. To understand the performance of these devices, the electronic structures at the interface between the pentacene and the dielectric layers were also studied. Therefore, the purpose of this study was to determine if replacing conventional SiO_2 with SiON improved performance in dielectric applications. In addition, the electronic structures at the interface between the pentacene and dielectric layers were examined to understand the dielectric performance characteristics. Chemical reactions and band bending at the interface were investigated using x-ray photoelectron spectroscopy (XPS). The shifts in vacuum level and in highest occupied molecular orbital (HOMO) level were examined through ultraviolet photoelectron spectroscopy (UPS). The electronic structure of organic/metal,[14] organic/insulator,[15] and organic/organic interfaces[16] has been studied by several research groups. In this study, detailed electronic structures of pentacene/SiO_2 and pentacene/SiON systems and complete energy level diagrams are described.

II. EXPERIMENT

Figure 1 shows the schematic cross sections of the devices used in the thin film transistors. Heavily doped silicon wafers with either a SiO_2-insulating layer of 4.5 nm thickness or a SiON-insulating layer of the same thickness were used as substrates. The 4.5 nm SiO_2 layers were grown using a plasma oxidation process on *p*-type Si wafers cleaned using the standard Radio Corporation of America method. The nitridation process was performed using a rf source (inductively coupled plasma, 13.56 MHz). The pressure and substrate temperature were fixed at 500 mTorr and 400 °C, respectively.[17] The thickness and chemical composition of each dielectric layer were determined using medium-energy ion scattering (MEIS) spectroscopy. Thermal evaporation of the 100 nm thick pentacene layer was conducted at 130 °C

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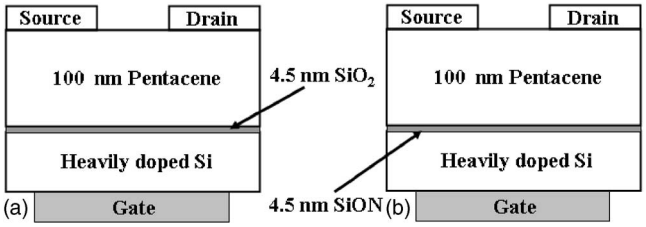

FIG. 1. Schematic device structure of the inverted-staggered pentacene thin film transistors (a) with a SiO_2 gate dielectric layer and (b) with a SiON gate dielectric layer.

under a base pressure of 1×10^{-9} Torr. The deposition rate was maintained at 0.1 Å/s. After the deposition of the pentacene layer, the sample was transferred to a metal deposition chamber. Without breaking the vacuum, gold source and drain electrodes were prepared at a thickness of 50 nm. The channel length and width of the pentacene TFTs were 50 and 1000 μm, respectively. The current-voltage behavior of the device was characterized in atmospheric air at room temperature using Keithley 2400 units.

To investigate the interface formation and the resulting electronic structures, pentacene was evaporated in a stepwise manner on sputter-cleaned SiO_2 and SiON substrates at room temperature. The deposition rate of pentacene was kept at 0.1 Å/s, and the accumulated layer thickness was monitored using a calibrated quartz thickness monitor. The background pressure of the preparation chamber was maintained at 1.4×10^{-9} Torr during film deposition. The valence band (sample bias: −15 V), C 1*s*, O 1*s*, N 1*s*, and Si 2*p* spectra were collected immediately after the deposition of each layer was complete. The XPS and UPS spectra were obtained on a PHI 5700 spectrometer using monochromatic Al $K\alpha$ (1486.6 eV) and He I (21.2 eV) sources. The base pressure of the analysis chamber was 2×10^{-10} Torr.

III. RESULTS AND DISCUSSION

A. The device characteristics for pentacene TFTs

The threshold voltage and mobility performance characteristics of the SiON and SiO_2 pentacene TFTs are shown in Figs. 2 and 3, respectively. Figure 2 displays the drain current–drain voltage curves (I_D-V_D) obtained for the

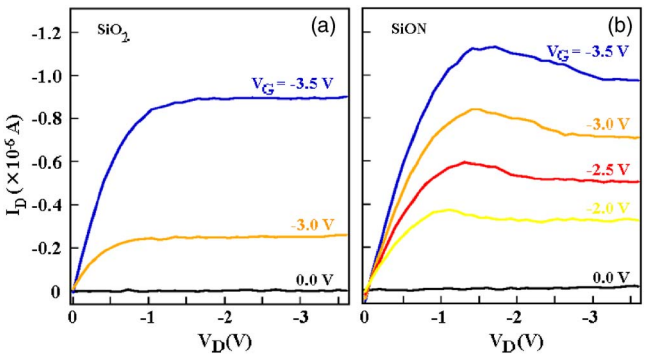

FIG. 2. (Color online) Field effect transistor characteristics of our pentacene TFTs: I_D-V_D curves at various V_G obtained from TFTs with (a) the SiO_2 gate dielectric layer and with (b) the SiON gate dielectric layer (channel length $L=50$ μm and width $W=1000$ μm).

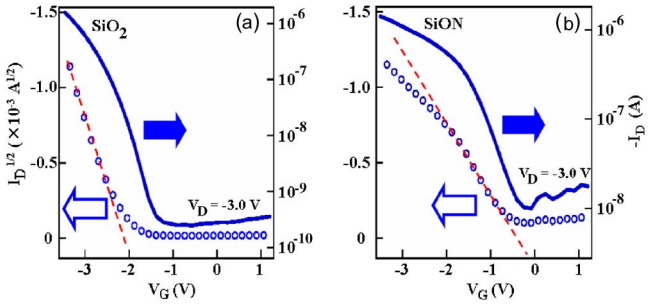

FIG. 3. (Color online) Field effect transistor characteristics of our pentacene TFTs: $\sqrt{I_D}$-V_G curves for the estimation of saturation regime mobility that were obtained at $V_D=-3$ V from TFTs with (a) the SiO_2 dielectric layer and with (b) the SiON dielectric layer (channel length $L=50$ μm and width $W=1000$ μm).

pentacene-based TFTs with ultrathin SiO_2 and SiON films as gate dielectric layers. The curves were typical for *p*-type OTFTs working in an accumulation mode. The SiON pentacene TFTs demonstrated desirable TFT characteristics at operating voltages less than −3 V, while the SiO_2 pentacene TFTs did not operate at less than −3 V. The maximum saturation current achieved over a gate bias (V_G) of −3 *V* from the SiON OTFT was much higher than that achieved by the SiO_2 dielectric layer.

The threshold voltages for the two pentacene TFTs were determined from $\sqrt{-I_D}$ vs V_G curves, as shown in Figs. 3(a) and 3(b). The SiON pentacene TFT had a threshold voltage of −0.45 V, much lower than the SiO_2 dielectric device (−2.5 V). The threshold voltage of the SiON dielectric device was comparable to that previously reported for low-voltage pentacene TFTs.[13,18,19] However, the large difference in threshold voltage between the SiON and SiO_2 devices could not be attributed to differences in dielectric constant, because the dielectric constant of SiON is not much higher (5.0–5.5) than that of SiO_2 (3.9). Thus, it was inferred that the electronic structures at the interface between the pentacene and dielectric layers affected the characteristics of the TFTs. The interfacial characteristics of the electronic structure were investigated using *in situ* UPS and XPS to determine the primary cause of the lower operating voltage. The measured field effect saturation mobilities were also determined from the $\sqrt{-I_D}$ vs V_G curves, as shown in Figs. 3(a) and 3(b). The SiON pentacene TFT had a lower mobility (0.07 cm^2/V s) than the device with the SiO_2 dielectric layer (0.3 cm^2/V s). The reason for the reduced mobility was the large number of charge trap sites at the interface between the pentacene and the SiON layers. As shown in Fig. 4 (MEIS spectra of SiON film), the nitride content was effectively localized on the film surface.[17] Therefore, the ON traps the carrier charge in a manner similar to the charge-trapping layer for nonvolatile memory.

B. The electronic structure of the pentacene/dielectric interfaces

The electronic structure at the interface between the pentacene and dielectric layers was investigated using *in situ* UPS and XPS. Figures 5 and 6 show the UPS spectra during deposition of pentacene on SiO_2 and SiON. The spectra

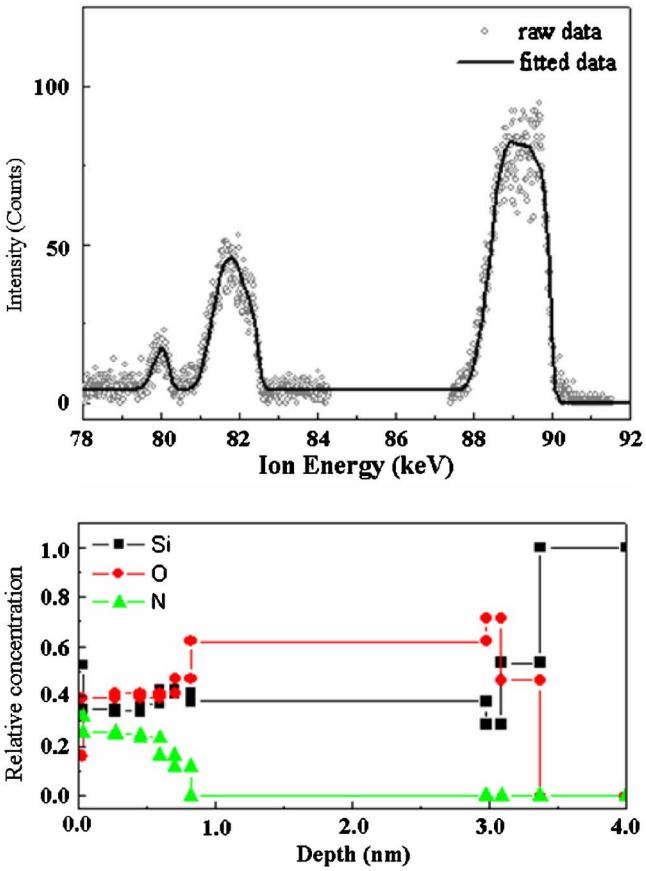

FIG. 4. (Color online) MEIS spectra of the SiON gate dielectric layer. The bottom part shows the depth-profiling data obtained from fitted MEIS spectra.

shown in Figs. 5(a) and 5(b) were collected in the secondary electron cutoff region for the SiO_2 and SiON layers, respectively. The secondary electron cutoff position noticeably moved to a higher binding energy upon deposition of 0.4 nm

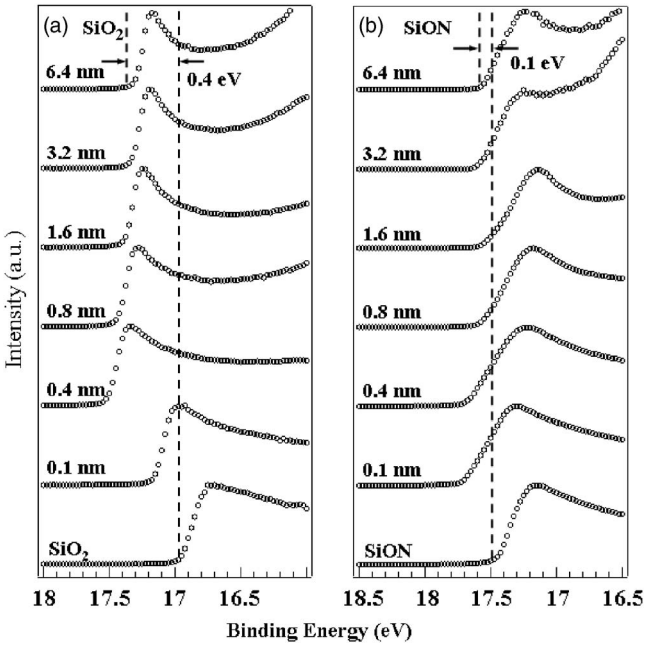

FIG. 5. The UPS spectra in the secondary cutoff region collected during the step-by-step layer deposition of pentacene on (a) the SiO_2 surface and on (b) the SiON surface.

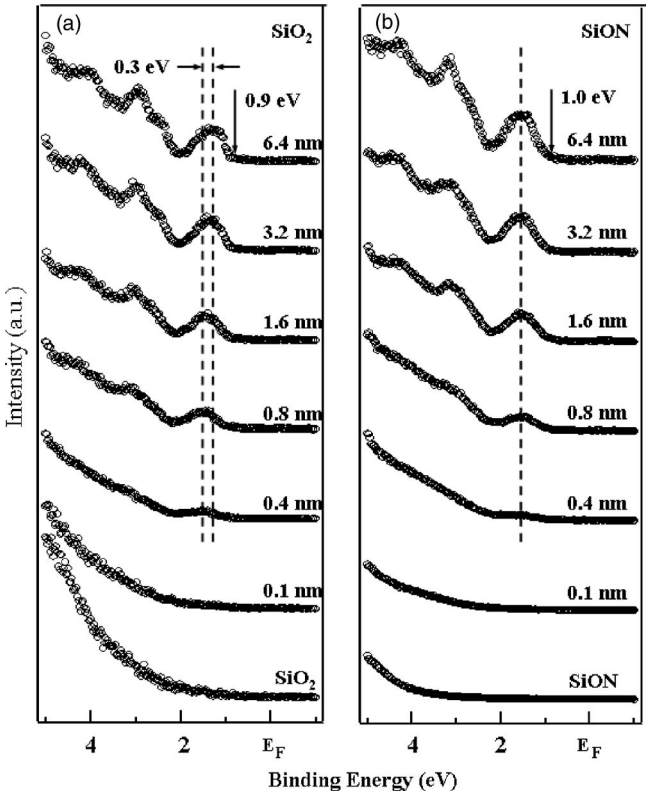

FIG. 6. The UPS spectra collected near the Fermi level as a function of pentacene deposition on (a) the SiO_2 surface and on (b) the SiON surface.

of pentacene. As more pentacene was deposited, the secondary electron cutoff position slightly shifted towards a lower binding energy. Similar results for other pentacene/dielectric interfaces have been previously reported.[15,20] Although the exact origin of this shift remains unclear, one of the most probable explanations which has been offered is the displacement of excess oxygen from the surface by deposition of the organic.[15] Removal of any oxygen adsorbates effectively reduces the surface work function. The difference in the cutoff position between the SiO_2 and SiON layers is clearly shown in Figs. 5(a) and 5(b). The total shift in the cutoff position toward a higher binding energy was 0.4 eV for the SiO_2 layer and 0.1 eV for the SiON layer. The change in position has been attributed to the formation of dipoles at the interface between the organic and the dielectric or metal layers because the formation of interface dipoles varies with the cutoff position as the thickness of the deposited organic layer increases.[21] Moreover, the secondary electron cutoff shift toward higher binding energies indicated a step down of the vacuum level from the inorganic to the organic film, consistent with a positive dipole,[22] suggesting the formation of an interface dipole with its negative pole pointing toward the substrate and its positive pole toward the organic layer.

Figures 6(a) and 6(b) show the evolution of HOMO onset during the growth of the pentacene layer on SiO_2 and SiON, respectively. When the coverage of pentacene was greater than 0.4 nm, the features of the pentacene layer were dominant. In addition, the HOMO of pentacene gradually shifted towards lower binding energies and the total shift was 0.3 eV for the pentacene/SiO_2 interface. This result confirmed the band bending at the pentacene/SiO_2 interface.

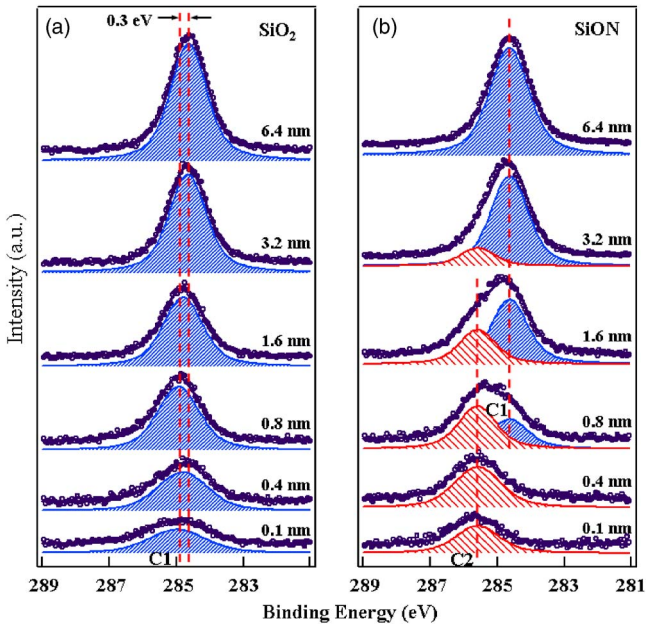

FIG. 7. (Color online) The core-level spectra of C 1*s* obtained during the pentacene deposition on (a) the SiO_2 surface and on (b) the SiON surface, respectively. Decompositions of the spectra by curve-fitting analyses are also shown, with different component marked by different shading.

The shift in HOMO onset was saturated as the thickness of the pentacene layer increased. The saturation point is occurred 0.9 eV below the Fermi level on the SiO_2 layer, based on the measurement of a sample with a 6.4 nm thick pentacene layer. On the other hand, as shown in Fig. 6(b), there was no shift in HOMO onset for the pentacene/SiON interface. The HOMO onset was measured at 1.0 eV for the SiON layer. No additional shift in the onset position was observed for either the SiO_2 or the SiON layer when the thickness of the pentacene layer was greater than 6.4 nm, indicating that the interaction between the pentacene and dielectric layer was confined to a short range and that no further interactions occurred as the pentacene layer thickened.

The core-level spectra of the sample were collected during step-by-step deposition to investigate band bending and chemical reaction between the layers. Figure 7 shows the core-level spectra of C 1*s*, obtained during pentacene deposition on the SiO_2 and SiON. The line shapes of these spectra were analyzed using a standard least-squares fitting scheme. Figure 7(a) reveals no reaction between the pentacene and the SiO_2 substrate. A noticeable shift of the C 1*s* core peak level (C1) toward lower binding energies was observed as the thickness of the pentacene layer thickness increased. The total C 1*s* peak shift was 0.3 eV, which was same as the shift of HOMO for the SiO_2 layer. These findings also confirmed band bending at the interface of the pentacene/SiO_2 (0.3 eV).[23] The band bending gradually was released with increasing distance from the interface. On the other hand, the C 1*s* spectra in Fig. 7(b) obtained during pentacene deposition on SiON consisted of two components. The position of one component (C1) corresponded with a pristine pentacene, and the other component (C2) exhibited a shift in binding energy of 0.92 eV due to the reaction between pentacene and SiON substrate. Band bending at the interface between pentacene and the SiON layer was not observed, consistent with the absence of change in HOMO [Fig. 6(b)]. The magnitude of the interface dipole, HOMO, and the lowest unoccupied molecular orbital (LUMO) offsets were determined by comparing the core-level spectra taken after deposition of each layer.[24] The interface dipoles obtained were 0.7 eV at the pentacene/SiO_2 interface and 0.1 eV at the pentacene/SiON interface after subtracting the contribution of band bending.

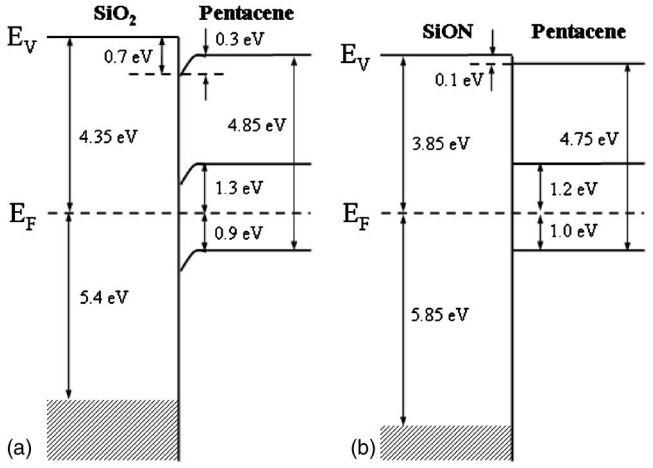

FIG. 8. Energy level diagram of pentacene on (a) the SiO_2 surface and on (b) the SiON surface. The magnitude of interface dipole at the pentacene/SiO2 interface is larger than that at the pentacene/SiON by 0.6 eV.

An energy diagram was constructed by combining the changes in spectra shown in Figs. 5–7. As shown Fig. 8, the energy gap between HOMO and LUMO was about 2.2 eV, as previously reported.[24] The ionization energy of pentacene was estimated to be about 4.75–4.85 eV, which agreed well with the expected value of 5.0 eV.[25] Generally, in an energy diagram, when a negative gate voltage is applied for the operation of the pentacene TFTs, the gate voltage bends HOMO levels towards the Fermi level. Therefore, mobile charge carriers accumulate and form a conducting channel. However, a positive interface dipole bends HOMO levels away from the Fermi level, decreasing hole density of the channel, as shown in Fig. 8(a). In other words, the positive interface dipole field modified the surface potential of the gate dielectric layer in a manner similar to that resulting from application of a positive gate voltage—the opposite operating voltage for *p*-type TFTs.[26] The magnitude of the positive interface dipole at the pentacene/SiO_2 interface was larger than that at the pentacene/SiON by 0.6 eV. The HOMO level of the pentacene on SiO_2 was bent away from the Fermi level by 0.3 eV. Therefore, the Fermi level was closer to the HOMO level of the pentacene/SiON interface than to the HOMO level of the pentacene/SiO_2 interface. Thus, it follows that the OTFTs with SiON gate dielectric layers had lower operating gate voltages and lower threshold voltages (−0.45 V versus −2.5 V) than the SiO_2 OTFTs.

IV. CONCLUSIONS

In conclusion, this paper describes the fabrication of pentacene-based TFTs with ultrathin (4.5 nm) SiO_2 and SiON gate insulator films. The device with SiON gate dielec-

tric layer had an operating gate voltage of less than −3.0 V and a threshold voltage of −0.45 V, which was lower than that of the SiO_2 device (−2.5 V). Electronic structures at the interface between the pentacene and dielectric layers were investigated by *in situ* UPS and XPS to determine the origin of the lower operating voltage. The magnitudes of dipole strength and band bending at the interface were determined and complete energy level diagrams for pentacene on SiO_2 and on SiON were constructed. The positive interface dipole field modified the surface potential of the gate dielectric layer in a manner similar to applying a positive gate voltage, which is the opposite operating voltage for *p*-type TFTs. The interface dipole modified the surface potential of the dielectric layer next to the transistor channel. Therefore, this study demonstrates that, in addition to the dielectric constant, the interface dipole also is an important factor for low-voltage operating OTFTs.

ACKNOWLEDGMENTS

This work was supported by BK21 project of the Korea Research Foundation (KRF) and the KOSEF, through National Core Research Center for Nanomedical Technology, the National Program for Tera-level Nanodevices of the Ministry of Science and Technology as one of the 21 century Frontier Programs and System IC 2010 project.

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