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Fabrication and characterization of the pentacene thin film transistor with a Gd_2O_3 gate insulator

S.J. Kang, K.B. Chung, D.S. Park, H.J. Kim, Y.K. Choi, M.H. Jang, M. Noh, C.N. Whang*

Institute of Physics and Applied Physics, Yonsei University, 134 Shinchon-dong, Sudaemoon-ku, Seoul 120-749, Korea

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Abstract

Pentacene thin film transistors (TFTs) on a high-κ Gd_2O_3 gate insulator layer were fabricated and characterized. The Gd_2O_3 layer was grown by ion beam assisted deposition (IBAD) on a heavily-doped silicon substrate in ultra high vacuum, where the measured dielectric constant of the oxide layer was about 7.4. The maximum field effect mobility and the on/off ratio of the TFTs were 0.1 cm^2/Vs and about 10^3, respectively. The threshold voltage of the device was dramatically decreased (15.3 V → −3.5 V) as the high-κ Gd_2O_3 layer replaced the SiO_2 layer.

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1. Introduction

Pentacene has been the most attractive material for organic thin film transistors (OTFTs), since its properties were known to be comparable to that of hydrogenated amorphous silicon thin film transistors (a-Si: H TFTs) [1,2]. Until now, many useful methods were developed to fabricate the optimized pentacene TFTs with highest field effect mobility. Normally, the silicon dioxide surface is modified via the octadecyltrichlorosilane (OTS) treatment before the pentacene layer deposition to improve interface and the properties of organic layer [3–6]. The post-annealing of pentacene layer facilitate grain growth, which decreases grain boundary density and results in the increased field effect mobility [7]. As we know, the highest field effect mobility value reported is 5 cm^2/Vs by T.W. Kelly [8]. The use of purified pentacene source is also crucial to minimize conduction via impurity level in device [9,10].

Although many progresses have been made, the pentacene TFTs still have problems. One of them is too high operation voltage to achieve applicable organic semiconductor devices. Regardless of its importance, effort to lower the operating voltage has been less attempted compared to improving the field effect mobility. Recently, researchers have tried to decrease the threshold voltage by using new gate dielectrics such as high-κ dielectrics or organic dielectrics. The device with a thin Al_2O_{3+x} gate dielectric layer delivered a little bit improved threshold voltage of about −10 V [11]. Choo et al. reported better threshold voltage of −5 V in a pentacene TFTs by adopting a thin SiN_x layer [12]. Another approach using organic dielectrics such as poly-chloro-*p*-xylylene and polyvinyl alcohol have been tried. Unfortunately, most of the known organic dielectrics have small dielectric constants and the pentacene TFTs using these layers have high threshold voltage of around −20 V [13,14]. The best threshold voltage reported was about −5 V by using PVP as a gate insulator [15].

Here, we report the pentacene TFTs using a thin high-κ Gd_2O_3 layer as a gate insulator to lower the threshold voltage. We also carefully studied and compared dielectric constant, field effect mobility, on/off ratio and threshold voltage of the three different pentacene TFTs. One was prepared on Gd_2O_3 and the other two was prepared on SiO_2 with and without post-annealing, respectively.

* Corresponding author. Tel.: +82 2 364 7941; fax: +82 2 312 7090.
E-mail address: cnwhang@yonsei.ac.kr (C.N. Whang).

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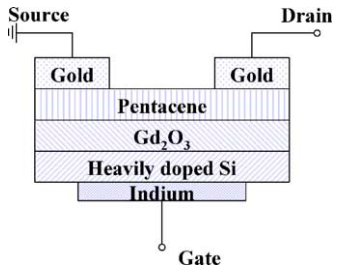

Fig. 1. Schematic diagram of pentacene TFTs used in this experiment. Top contact structure was adopted. The device had a top contact structure with a 200 nm thick pentacene layer on a 280 nm thick Gd_2O_3 layer.

2. Experiment

The typical structure of Pentacene TFTs used in this experiment is shown in Fig. 1. Heavily-doped silicon wafers were cleaned chemically before growing the Gd_2O_3 layer by using the standard RCA method, which removed organic and metallic residues from the surface [16,17]. After the RCA cleaning, silicon wafers were dipped in a dilute HF solution for removing the natural SiO_2 layer in order to obtain the clean silicon surface. Cleaned silicon wafers were introduced into the UHV growth chamber and evacuated to low 6.5×10^{-8} Pa. The gadolinium metal was evaporated on the prepared silicon surface via ionized beam assisted deposition (IBAD). For the formation of Gd_2O_3 layer, oxygen gas was introduced into the chamber up to a partial pressure of 7.9×10^{-4} Pa and ionized with oxygen gun at the acceleration voltage of 1.7 kV during the growth. The deposition rate was maintained at 0.04 nm/s and the substrate temperature was kept at room temperature. The final thickness of the Gd_2O_3 layer was confirmed by using the ellipsometry technique.

The 200 nm thick pentacene active layer was thermally evaporated on the prepared Gd_2O_3 layer in the organic deposition chamber kept at the pressure below 1.33×10^{-7} Pa. The deposition rate for pentacene was maintained at 0.01 nm/s at the evaporation temperature of about 130 °C in our system, where a significant decrease of thermal dissociation of pentacene molecules was expected. We used as-received Aldrich pentacene with 97% purity without additional purification. After the pentacene layer deposition, sample was moved to the metal deposition chamber without breaking the vacuum for the formation of the 50 nm thick source and drain electrodes of gold. The channel length and width in our pentacene TFTs were 50 and 1000 μm, respectively.

The crystalline quality of the Gd_2O_3 layer was characterized by in-situ reflection high-energy electron diffraction (RHEED). The electrical properties of the Gd_2O_3 layer were checked by capacitance–voltage measurement (HP 4280A capacitance meter). The structural properties of the pentacene layer were investigated by using atomic force microscopy (AFM) and the high-resolution synchrotron X-ray diffraction (XRD) facility at the Pohang Light Source (PLS). The study of current–voltage characteristics on the pentacene TFTs was done by using a Keithley 4200-SCS source measurement unit.

3. Results and discussion

Fig. 2 showing the RHEED pattern from the 280 nm thick Gd_2O_3 layer confirms amorphous phase of the film. The inset graph of Fig. 2 exhibits the capacitance–voltage characteristics of 90, 190, and 280 nm thick Gd_2O_3 films, respectively. The dielectric constant of 280 nm thick Gd_2O_3 layer was determined as 7.4 from the C–V plots, smaller than the previous reports of Gd_2O_3 (∼11) [18,19]. It seems to be attributed to the amorphous phase of our Gd_2O_3 layer. The current density and breakdown voltage for 280 nm thick Gd_2O_3 layer was about 10^{-3} A/cm^2 at the field strength of −0.3 Mv/cm.

The crystalline structure of the pentacene film on the Gd_2O_3 dielectric layer was investigated by using the high-resolution synchrotron XRD facility at the Pohang Light Source (PLS). All the diffraction peaks appeared in Fig. 3(a) correspond to the (0 0 *l*) Bragg's peaks of the pentacene, showing the well-developed single-phase pentacene film of the thin film phase. Our previous study suggested that it was mainly due to the film formation at low deposition rate in ultra high vacuum conditions [20]. From the Bragg's peaks appeared at 5.73°, 11.47°, 17.21°, 23.03° and 28.83° in 2θ, we can accurately determine the repeat unit of 15.46 Å ± 0.06 Å. Considering the well-known *c*-axis lattice constant of the pentacene molecule [21,22], the tilting angle of the pentacene molecules on Gd_2O_3 layer is 15.1° from the upright position, whereas it was 15.5° on SiO_2 layer [7]. Additional study on the same sample was done by using AFM in tapping mode. Fig. 3(b), obtained from the 200 nm thick pentacene film on Gd_2O_3 dielectric layer, reveals polycrystalline feature of the film. The average grain size of the polycrystalline pentacene film was about 190 nm. Reminding the results of the

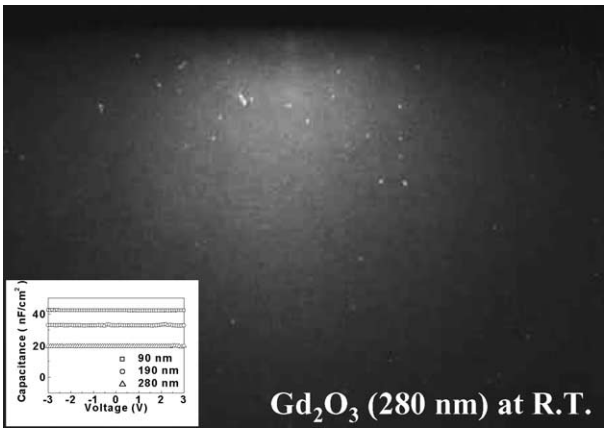

Fig. 2. The RHEED pattern, taken from the Gd_2O_3, indicates amorphous phase of the film grown on clean silicon (1 0 0) surface at room temperature. The C–V plots are shown in inset.

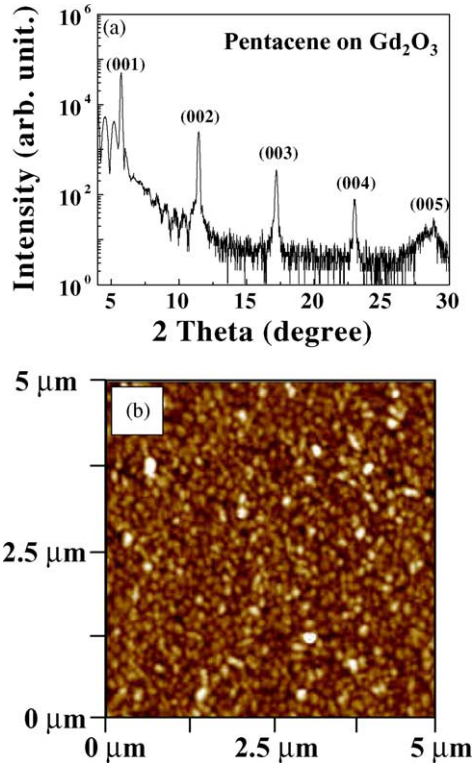

Fig. 3. (a) The high-resolution synchrotron X-ray diffraction pattern taken from the pentacene layer on the Gd_2O_3 layer. (b) The AFM image of pentacene film on a Gd_2O_3 gate oxide layer.

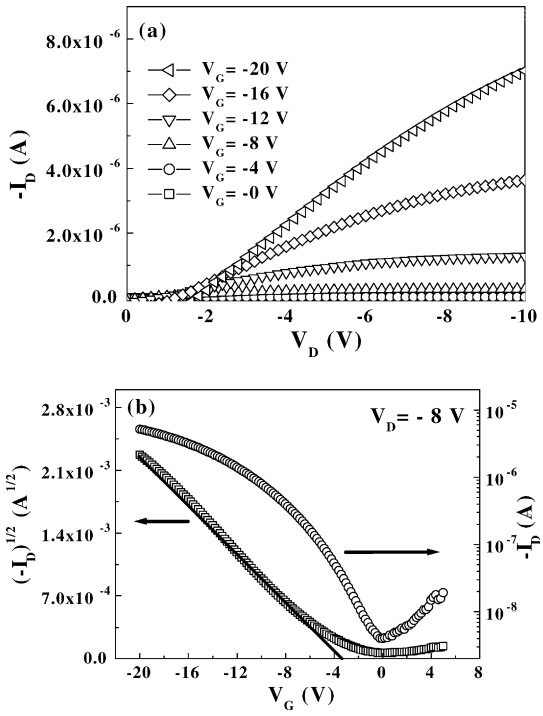

Fig. 4. (a) Drain current–drain voltage characteristics of the pentacene TFTs on a thin high-κ Gd_2O_3 layer, where the channel width was 1000 μm and the channel length was 50 μm. (b) Drain current (right *y*-axis) and the square root of drain current (left *y*-axis) vs. gate voltage plot for the $V_D = -8$ V.

film on SiO_2 layer [7], the average size of pentacene domains on a Gd_2O_3 dielectric layer is little bit smaller and rougher.

Fig. 4 shows the measured electrical properties of the pentacene TFTs with a thin high-κ Gd_2O_3 gate insulator, where the 200 nm thick pentacene active layer has a 1000 μm channel width and a 50 μm channel length. Fig. 4(a) shows plots of drain current (I_D) versus drain voltage (V_D) at the various gate voltages (V_G). The observed current–voltage behavior is similar to those of a typical p-type transistor. The I_D–V_D plots comply with the well-known I_D–V_D characteristics [23,24].

$$I_D = \frac{WC_i}{2L}\mu(V_G - V_T)^2 \quad (1)$$

where, W is the channel width, L is the channel length, μ is the mobility, V_T is the threshold voltage and C_i is the capacitance of the thermally grown 280 nm thick Gd_2O_3 film. By using this equation, the field effect mobility of 0.1 cm^2/Vs was obtained for $V_D = -8$ V. The inferior mobility to that of pentacene TFT on SiO_2 is attributed to the smaller domain size of the pentacene layer on Gd_2O_3. Fig. 4(b), showing the plots of drain current (I_D) and the square root of drain current versus gate voltage (V_G) for $V_D = -8$ V, exhibits a typical I_D–V_G feature of a transistor. The obtained threshold voltage was −3.5 V, dramatically decreased value compare to that of the TFTs on SiO_2 gate insulator as expected. Normally, quite a large threshold voltage was resulted in pentacene OTFTs using SiO_2 oxide layer. It could be reduced a little bit after the optimized post-annealing process [7]. One interesting result was reported by D.J. Gundlach, where a small and negative threshold voltage (−2 V) was observed at the device prepared on OTS-treated SiO_2 layer [25]. Interestingly, we obtained a similarly small and negative threshold voltage from the pentacene OTFTs using Gd_2O_3 instead of SiO_2 without OTS treatment on oxide layer. These results indicate that the use of high-κ gate insulator in OTFTs can be an interesting issue for achieving applicable organic semiconductor devices. Additional study is necessary to understand this feature further.

The on/off current ratio of about 10^3, obtained from the plot in Fig. 4 (b), is much smaller compared to the previous reports for pentacene OTFTs [3–5,9]. Being reminded that other researchers have used purified pentacene by vacuum gradient sublimation, we instead used unpurified 97% purity pentacene source material in our experiment. We suggested previously that the observed huge leakage current value (~10^{-8} A) between the drain and the source even at the off-state of device is attributed to the conduction via impurity levels originated from the structural isomers of pentacene [7]. We obtained one-order improved on/off ratio value by simply using the purified pentacene source.

We summarized dielectric constant, field effect mobility, on/off ratio and the threshold voltage in the Table 1 for structurally identical pentacene TFTs prepared on Gd_2O_3 and SiO_2 with and without post-annealing, respectively.

Table 1
The summary of dielectric constant, field effect mobility, on/off ratio and the threshold voltage of identical pentacene TFTs on a different gate oxide layer

Gate insulator	Dielectric constant	Mobility (cm^2/Vs)	On/off ratio	Threshold voltage (V)
Gd_2O_3 (280 nm)	7	0.1	10^3	−3.5
SiO_2 (100 nm)	3.9	0.19	10^3	15.3
SiO_2 (100 nm) post-annealing of pentacene layer	3.9	0.49	10^3	12.8

4. Conclusion

We fabricated and characterized pentacene thin film transistors (TFTs) on a high-κ Gd_2O_3 gate insulator layer. The RHEED pattern reveals that the thin Gd_2O_3 film was amorphous. The dielectric constant of the thin Gd_2O_3 film was about 7.4, decided from the C–V plots. The XRD data indicated that the pentacene molecules packed in parallel, stood upright with a tilting angle of 15.1°on the Gd_2O_3 gate insulator layer. The AFM image showed that the pentacene layer on Gd_2O_3 was in a polycrystalline phase. The obtained field effect mobility was 0.1 cm^2/Vs and the on/off ratio was about 10^3 for the pentacene TFTs on the Gd_2O_3 gate insulator. We observed huge decrease of the threshold voltage (15.3 V → −3.5 V) as the SiO_2 layer was replaced by the high-κ Gd_2O_3 layer.

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References

[1] J.M. Shaw, P.F. Seidler, IBM J. RES & DEV. 45 (2001) 3.
[2] C.D. Dimitrakopoulos, D.J. Mascaro, IBM J. RES & DEV. 45 (2001) 11.
[3] D. Knipp, R.A. Street, A. Volkel, J. Ho, J. Appl. Physiol. 93 (2003) 347.
[4] Y.Y. Lin, D.J. Gundlach, S.F. Nelson, T.N. Jackson, IEEE Electron Device Lett. 18 (1997) 606.
[5] M. Shtein, J. Mapel, J.B. Benziger, S.R. Forrest, Appl. Phys. Lett. 81 (2002) 268.
[6] C.K. Song, B.W. Koo, S.B. Lee, D.H. Kim, Jpn. J. Appl. Phys., Part I 41 (2002) 2730.
[7] S.J. Kang, M. Noh, D.S. Park, H.J. Kim, C.N. Whang, C.H. Chang, J. Appl. Physiol. 95 (2004) 2293.
[8] T.W. Kelly, et al., MRS Symp. Proc. 771 (1999) 169.
[9] C.D. Dimitrakopoulos, A.R. Brown, A. Pomp, J. Appl. Physiol. 80 (1996) 2501.
[10] D.J. Gundlach, Y.Y. Lin, T.N. Jackson, S.F. Nelson, D.G. Schlom, IEEE Electron Device Lett. 18 (1997) 87.
[11] J. Lee, J.H. Kim, S. Im, Appl. Phys. Lett. 83 (2003) 2689.
[12] M.H. Choo, W.S. Hong, S. Im, Thin Solid Films 420-421 (2002) 492.
[13] E. Becker, R. Parashkov, G. Ginev, D. Schneider, S. Hartmann, F. Brunetti, T. Dobbertin, D. Metzdorf, T. Riedl, H.H. Johannes, W. Kowalsky, Appl. Phys. Lett. 83 (2003) 4044.
[14] T. Yasuda, K. Fujita, H. Nakashima, T. Tsutsui, Jpn. J. Appl. Phys., Part I 42 (2003) 6614.
[15] H. Klauk, M. Halik, U. Zschieschang, G. Schmid, W. Radlik, W. Weber, J. Appl. Phys. 92 (2002) 5259.
[16] W. Keren, RCA Rev. 31 (1970) 207.
[17] W. Keren, RCA Rev. 31 (1970) 235.
[18] J.W. Johnson, B. Luo, F. Ren, B.P. Gila, W. Krishnamoorthy, C.R. Abernathy, S.J. Pearton, J.I. Chyi, T.E. Nee, C.M. Lee, C.C. Chuo, Appl. Phys. Lett. 77 (2000) 3230.
[19] J.W. Johnson, B.P. Gila, B. Luo, K.P. Lee, C.R. Abernathy, S.J. Pearton, J.I. Chyi, T.E. Nee, C.M. Lee, C.C. Chuo, F. Ren, J. Electrochem. Soc. 148 (2001) G303.
[20] S. J. Kang, D. S. Park, M. Noh, C. N. Whang, Korean Physics Society Conference, 406 (2002).
[21] R.W.G. Wyckoff, Crystal Structures, 2nd ed. (Interscience, New York 1971), Vol. 6, Part 2, p. 519.
[22] R.B. Campbell, J. Monteath Robertson, J. Trotter, Acta Crystallogr. 14 (1961) 705.
[23] G. Horowitz, Adv. Mater. 10 (1998) 365.
[24] D.A. Neamen, Semiconductor Physics & Devices, 2nd edn., Irwin McGraw-Hill, New York, 1997.
[25] D.J. Gundlach, H. Klauk, C. D. Sheraw, C. Kuo, J. Huang and T. N. Jackson, 1999 IEDM Tech. Digest 111 (1999).