Journal of the Korean Physical Society, Vol. 45, No. 4, October 2004, pp. 935∼938

# Characterization of a Pentacene Thin-Film Transistor with a $HfO_2/Al_2O_3$ Gate Insulator

H. J. Kim, S. J. Kang, D. S. Park, K. B. Chung, M. Noh and C. N. Whang*
*Institute of Physics and Applied Physics, Yonsei University, Seoul 120-749*

M. H. Cho
*Nano-surface Group, Korea Research Institute of Standards and Science, Daejon 305-600*

(Received 28 June 2004)

We fabricated pentacene thin-film transistors on $HfO_2/Al_2O_3$ gate insulator layers in an ultra-high vacuum system for the first time. The $HfO_2/Al_2O_3$ was used as a gate insulator to decrease the operating voltage of the pentacene thin-film transistors. The field-effect mobility of the devices with $HfO_2/Al_2O_3$ was obtained by using the I-V characteristics, and the value was 0.024 $cm^2/Vs$. The threshold voltage of the pentacene thin-film transistors with $HfO_2/Al_2O_3$ was decreased dramatically compared to that for devices using $SiO_2$ (15.3 $\rightarrow -$ 0.25 V). Therefore, a thin $HfO_2/Al_2O_3$ gate insulator layer can be used in pentacene thin-film transistors to lower the operating voltage.

PACS numbers: 61.66.Hg, 73.61.Ph, 85.30.De, 85.30.Tv
Keywords: Pentacene, Thin-film transistors, Threshold voltage

## I. INTRODUCTION

Pentacene has been the most attractive material for organic thin-film transistors (OTFTs) because its properties are known to be comparable to those of hydrogenated amorphous silicon thin-film transistors (a-Si : H TFTs) [1,2]. Until now, many useful methods have been developed to fabricate optimized pentacene TFTs with the highest field-effect mobility. Normally, the silicon-dioxide surface is modified via an octadecyltrichlorosilane (OTS) treatment before the pentacene-layer deposition to improve the interface and the organic layer properties [3–6]. Post-annealing of the pentacene layer facilitates grain growth, which decreases the grain boundary density and increases the field-effect mobility [7]. The use of a purified pentacene source is also crucial to minimize conduction via impurity levels in the device [8,9]. The highest value of field-effect mobility is 2.1 $cm^2/Vs$, which was reported by Jackson's group [10].

Although much progress has been made, pentacene TFTs still have problems. One is that the operating voltage is still too high to achieve useful organic semiconductor devices. Regardless of its importance, fewer studies have been aimed at lowering the operating voltage than have been aimed at improving the field-effect mobility. Recently, researchers tried to decrease the threshold voltage by using new gate dielectrics, such as high-$\kappa$ dielectrics or organic dielectrics. Though adopting a thin $Al_2O_{3+x}$ gate dielectric layer delivered an improved threshold voltage of about $-$ 10 V, it was still high [11]. Choo *et al.* reported a better threshold voltage of $-$ 5 V in a pentacene TFTs using thin $SiN_x$ [12]. Other approaches using organic dielectrics, such as poly-chloro-*p*-xylylene and polyvinyl alcohol, have been studied. Unfortunately, to now, most of the known organic dielectrics have had small dielectric constants, and the pentacene TFTs using these layers have had high threshold voltages of around $-$ 20 V [13,14].

Here, we report pentacene TFTs with a thin $HfO_2/Al_2O_3$ layer as a gate insulator to lower the threshold voltage. We carefully studied and compared the dielectric constants, the field-effect mobilities, the on/off ratios, and the threshold voltages of the two different pentacene TFTs, one on a $HfO_2/Al_2O_3$ gate insulator layer and the other on a $SiO_2$ gate insulator layer.

## II. EXPERIMENT

The typical structure of the pentacene TFTs used in this experiment is shown in Fig. 1. We fabricated pentacene thin-film transistors on a $HfO_2/Al_2O_3$ gate dielectric. Heavily doped Si substrates were chemically cleaned using the RCA method and dipped in dilute HF to remove metallic residue and native oxide [15,16]. $HfO_2/Al_2O_3$ insulator layers were grown at 300 °C by using alternating surface saturating reactions in a hot-wall-type, high-vacuum atomic layer deposition (ALD)

*E-mail: cnwhang@yonsei.ac.kr

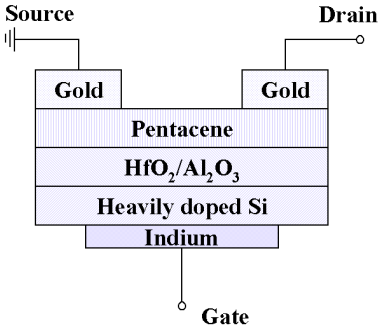


Fig. 1. Schematic diagram of the pentacene TFTs used in this experiment. The device had a top contact structure with a 100-nm-thick pentacene layer on a 3-nm thin $HfO_2/Al_2O_3$ layer.

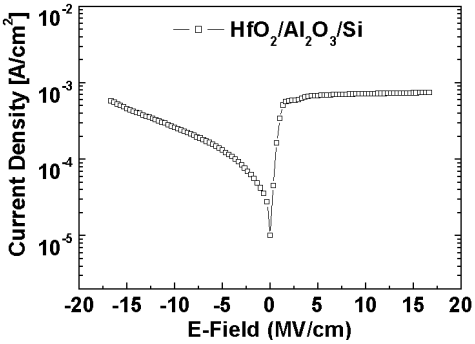


Fig. 2. Plot of the current density versus electric field for the $Au/HfO_2/Al_2O_3/Si$ (heavily doped) structure.

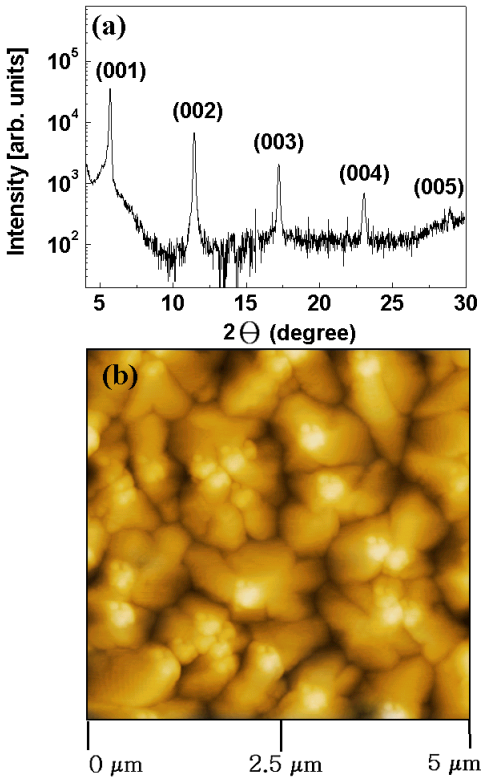


Fig. 3. (a) X-ray diffraction pattern taken from the pentacene layer on a $HfO_2/Al_2O_3$ layer. (b) The AFM image of the pentacene film on a $HfO_2/Al_2O_3$ gate oxide layer.

chamber [17]. At first, $Al_2O_3$ films were grown on a Si substrate using TMA (Trimethtylalminum $[Al(CH_3)_3]$) and $H_2O$ at a growth rate of 1.05 Å/cycles. After the growth of $Al_2O_3$ with a 1-nm film thickness, $HfO_2$ films were deposited on the $Al_2O_3/Si$ heterostructures by using a precursor of $HfCl_4$ and $H_2O$ at a growth rate of 0.8 Å/cycles until a 2-nm film thickness had been achieved. $N_2$ gas was supplied as the purge and the carrier gas for the processes to deposit the $Al_2O_3$ and the $HfO_2$ insulator layers via ALD.

A 100-nm-thick pentacene active layer was thermally evaporated onto the prepared $HfO_2/Al_2O_3$ layer at a chamber pressure lower than $2.0 \times 10^{-9}$ Torr. The deposition rate for pentacene was maintained at 0.1 Å/s with an evaporation temperature of about 180 °C in our system. We used as-received Aldrich pentacene with 97 % purity without additional purification. After the pentacene layer deposition, the sample was moved from the organic deposition chamber to the metal deposition chamber without breaking the vacuum for the formation of 50-nm-thick source and drain electrodes of gold. The channel length and width in our pentacene TFTs were 50 $\mu$m and 1000 $\mu$m, respectively.

The electrical properties of the $HfO_2/Al_2O_3$ layer were studied by using capacitance-voltage measurements (HP 4280A capacitance meter). The structural properties of the pentacene layer were investigated by using atomic force microscopy (AFM) and X-ray diffraction (XRD). The study of current-voltage characteristics for the pentacene TFTs was done by using a Keithley 4200-SCS source measurement unit.

## III. RESULTS AND DISCUSSION

Figure 2 exhibits the current density versus electric field characteristics measured from the $Au/HfO_2/Al_2O_3/Si$ (heavily doped) structure. The breakdown field of the $HfO_2/Al_2O_3$ insulator layer was measured to be 0.3 MV/cm. The leakage current density was about $1 \times 10^{-4}$ A/cm$^2$ at a gate-source bias of $-3$ V. In comparison to the values for $SiO_2$, this breakdown field was slightly lower and the leakage current was large. Considering the thickness of our oxide (3 nm), $HfO_2/Al_2O_3$ was very useful in the breakdown field and the leakage current for the gate insulator. The dielectric constant of our thin $HfO_2/Al_2O_3$ film was measured to be 3.29. The dielectric constant is smaller than previously reported values, due to the double layers and the thickness of the $HfO_2/Al_2O_3$ (3 nm).

The crystalline structure of the pentacene film on the $HfO_2/Al_2O_3$ dielectric layer was investigated by using XRD. All the diffraction peaks appearing in Fig. 3(a)

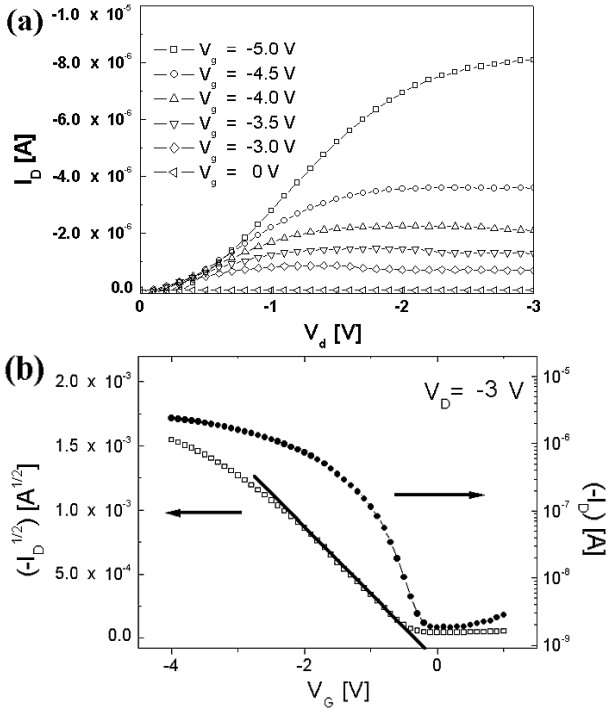


Fig. 4. (a) Drain current-drain voltage characteristics of the pentacene TFTs on thin $HfO_2/Al_2O_3$ layers, where the channel width was 1000 $\mu$m and the channel length was 50 $\mu$m. (b) Drain current (right $y$-axis) and the square root of the drain current (left $y$-axis) vs. gate voltage for $V_D = -3$ V.

correspond to the (00$l$) Bragg peaks of the pentacene, showing a well-developed single-phase pentacene film with a thin-film phase, which our previous study suggested was mainly due to the film formation at a low deposition rate in an ultra-high vacuum [18]. From the Bragg peaks appearing at 5.68°, 11.46°, 17.22°, 23.06°, and 28.90° in the $2\theta$ scan, we accurately determined the repeat-unit length to be 15.43 ± 0.07 Å. If the well-known $c$-axis lattice constant of the pentacene molecule is considered [19, 20], the tilt angle of the pentacene molecules on $HfO_2/Al_2O_3$ layer was 15.41° from the upright position whereas it was 15.5° on $SiO_2$ layer [7]. Additional study on the same sample was done by using AFM in the tapping mode. Figure 3(b), obtained from the 100-nm-thick pentacene film on a $HfO_2/Al_2O_3$ dielectric layer, reveals a polycrystalline feature. The average grain size of the polycrystalline pentacene film was about 1.5 $\mu$m. In comparison to the results for a pentacene film on a $SiO_2$ layer [7], the average size of the pentacene domains on a $HfO_2/Al_2O_3$ dielectric layer is dramatically increased.

Figure 4 shows the measured electrical properties of the pentacene TFTs with a thin $HfO_2/Al_2O_3$ gate insulator, where the 100-nm-thick pentacene active layer had a 1000-$\mu$m channel width and a 50-$\mu$m channel length. Figure 4(a) shows plots of drain current ($I_D$) versus drain voltage ($V_D$) at various gate voltages ($V_G$). The observed

Table 1. Summary of the dielectric constant, the field-effect mobility, the on/off ratio, and the threshold voltage of identical pentacene TFTs on different gate oxide layers.

| Gate insulator | Dielectric constant | Mobility [$cm^2$/Vs] | On/off ratio | Threshold voltage [V] |
|---|---|---|---|---|
| $HfO_2/Al_2O_3$ (2 nm/1 nm) | 3.29 | 0.024 | $10^2$ | −0.25 |
| $SiO_2$ (100 nm) | 3.9 | 0.19 | $10^3$ | 15.3 |

current-voltage behaviors are similar to those of a typical p-type transistor. The $I_D$-$V_D$ plots agree with the well-known formula [21,22]

$$I_D = \frac{WC_i}{2L}\mu(V_G - V_T)^2, \quad (1)$$

where $W$ is the channel width, $L$ is the channel length, $\mu$ is the mobility, $V_T$ is the threshold voltage, and $C_i$ is the capacitance of the 3-nm thin $HfO_2/Al_2O_3$ film. With this equation, a field-effect mobility of 0.024 $cm^2$/Vs was obtained for $V_D = -3$ V. Figure 4(b), showing plots of the drain current ($I_D$) and the square root of the drain current versus the gate voltage ($V_G$) for $V_D = 3$ V, exhibits the typical $I_D$-$V_G$ behavior of a transistor. The obtained threshold voltage was − 0.25 V, dramatically decreased compared to that for TFTs on a $SiO_2$ gate insulator, as expected. The threshold voltages of pentacene TFTs on a $SiO_2$ gate insulator are still high even after an optimized post-annealing process [7]. These results indicate that lowering the operation voltage of a device is possible by adopting a thin $HfO_2/Al_2O_3$ gate insulator, which is advantageous for achieving useful organic semiconductor devices.

The on/off current ratio of about $10^2$ obtained from the plot in Fig. 4(b) is much smaller compared to the previous reports for pentacene OTFTs [3–5,9]. Although other researchers have used pentacene purified by employing vacuum gradient sublimation, we used an unpurified 97 %-pure pentacene source material in our experiment. We suggested previously that the observed huge leakage current values ($\sim 10^{-8}$ A) between the drain and the source even in the off-state of the device could be attributed to conduction via impurity levels originating from structural isomers of pentacene [7]. A summary of the dielectric constants, the field effect mobilities, the on/off ratios, and the threshold voltages of identical pentacene TFTs on two different gate oxide layers are shown in table 1 for $HfO_2/Al_2O_3$ and $SiO_2$ layer.

## IV. CONCLUSION

We fabricated and characterized pentacene thin film transistors (TFTs) on thin $HfO_2/Al_2O_3$ gate insulator layers for the first time. The dielectric constant of the thin $HfO_2/Al_2O_3$ film was about 3.29. The XRD data

indicated that the pentacene molecules were packed in parallel and stood upright with a tilting angle of 15.41° on the $HfO_2/Al_2O_3$ gate insulator layer. The AFM image showed that the grain size of the pentacene on $HfO_2/Al_2O_3$ was increased dramatically. Compared to that of the pentacene on $SiO_2$ the obtained field effect mobility was 0.024 $cm^2$/Vs, and the on/off ratio was about 102 for the pentacene TFTs on thin $HfO_2/Al_2O_3$ gate insulators. We observed a huge decrease in the threshold voltage (15.3 $\rightarrow -$ 0.25 V) when a thin $HfO_2/Al_2O_3$ layer was used instead of a $SiO_2$ layer.

## ACKNOWLEDGMENTS

This work was supported by the BK21 project of the Korea Research Foundation (KRF). Additional support by the Yonsei Center for Nano Technology (YCNT) is gratefully acknowledged.

## REFERENCES

[1] J. M. Shaw and P. F. Seidler, IBM J. RES & DEV. **45**, 3 (2001).
[2] C. D. Dimitrakopoulos and D. J. Mascaro, IBM J. RES & DEV. **45**, 11 (2001).
[3] D. Knipp, R. A. Street, A. Volkel and J. Ho, J. Appl. Phys. **93**, 347 (2003).
[4] D. Knipp and R. A. Street, J. Non-Crys. Sol. **338**, 595 (2004).
[5] M. Shtein, J. Mapel, J. B. Benziger and S. R. Forrest, Appl. Phys. Lett. **81**, 268 (2002).
[6] C. K. Song, B. W. Koo, S. B. Lee and D. H. Kim, Jpn. J. Appl. Phys. Part I, **41**, 2730 (2002).
[7] S. J. Kang, M. Noh, D. S. Park, H. J. Kim, C. N. Whang and C. H. Chang, J. Appl. Phys. **95**, 2293 (2004).
[8] C. D. Dimitrakopoulos, A. R. Brown and A. Pomp, J. Appl. Phys. **80**, 2501 (1996).
[9] Yun-Myoung Kim, Sang-Woo Pyo, Jung-Soo Kim, Jae-Hoon Shim, Chung-Ha Suh and Young-Kwan Kim, Opt. Mat. **21**, 425 (2002).
[10] D. J. Gundlach, C. C. Kuo, S. F. Nelson and T. N. Jackson, *57$^{th}$ Annual Device Research Conference Digest*, (Santa Barbara, 1999). p. 164.
[11] J. Lee, J. H. Kim and S. Im, Appl. Phys. Lett. **83**, 2689 (2003).
[12] M. H. Choo, W. S. Hong and S. Im, Thin Solid Films **420**, 492 (2002).
[13] E. Becker, R. Parashkov, G. Ginev, D. Schneider, S. Hartmann, F. Brunetti, T. Dobbertin, D. Metzdorf, T. Riedl, H. H. Johannes and W. Kowalsky, Appl. Phys. Lett. **83**, 4044 (2003).
[14] T. Yasuda, K. Fujita, H. Nakashima and T. Tsutsui, Jpn. J. Appl. Phys. Part I, **42**, 6614 (2003).
[15] W. Keren, RCA Rev. **31**, 207 (1970).
[16] W. Keren, RCA Rev. **31**, 235 (1970).
[17] K. Kukli, M. Ritala and M. Leskela, Electrochem. Soc. Proc. **97**, 1137 (1997).
[18] S. J. Kang, D. S. Park, M. Noh and C. N. Whang, *Korean Physics Society Conference*, (Seoul, 2004). p. 406.
[19] R. W. G. Wyckoff, *Crystal Structures*, 2$^{nd}$ ed. (Interscience, New York, 1971), **6**, Part 2, p. 519.
[20] R. B. Campbell, J. Monteath Robertson and J. Trotter, Acta Crystallogr. **14**, 705 (1961).
[21] G. Horowitz, Adv. Mat. **10**, 365 (1998).
[22] D. A. Neamen, *Semiconductor Physics & Devices, 2$^{nd}$* (Irwin McGraw-Hill, New York, 1997), p. 456.